IN THE CLAIMS

1. (twice amended) A two-bit non-volatile memory transistor comprising:

a semiconductor region having a first conductivity type;

a first source/drain region located in the semiconductor region, the first source/drain region having a second conductivity type, opposite the first conductivity type;

a second source/drain region located in the semiconductor region, the second source/drain region having the second conductivity type, wherein a channel region of the first conductivity type is located between the first and second source/drain regions;

a gate dielectric layer located over the channel region and portions of the first and second source/drain regions;

a first floating gate electrode located on the gate dielectric layer over the channel region and the first source/drain region, wherein the first floating gate electrode has a first edge that is substantially vertical with respect to an upper surface of the semiconductor region, and wherein the first floating gate electrode stores charge representative of a first data bit;

a second floating gate electrode located on the gate dielectric layer over the channel region and the second source/drain region, wherein the second floating gate electrode has a second edge that is substantially vertical with respect to the upper surface of the semiconductor region, the second edge located adjacent

to the first edge, wherein the first and second edges define [floating gate electrodes are separated by] a gap over the channel region, and wherein the second floating gate electrode stores charge representative of a second data bit;

a dielectric layer located over the first floating gate electrode and the second floating gate electrode, including the first and second substantially vertical sidewalls; and

a control gate located over the dielectric layer, wherein a first portion of the control gate extends into the gap between the first and second edges [floating gate electrodes], wherein the first portion of the control gate is separated from the channel region by the dielectric layer and the gate dielectric layer.

2. (original) The 2-bit non-volatile memory transistor of Claim 1, wherein the first and second floating gate electrodes comprise polysilicon.

3. (original) The 2-bit non-volatile memory transistor of Claim 1, further comprising:

a first diffusion bit line continuous with the first source/drain region; and

a second diffusion bit line continuous with the second source/drain region.

4. (original0 The 2-bit non-volatile memory transistor of Claim 3, further comprising:

a first oxide region located over the first diffusion bit line; and

a second oxide region located over the second diffusion bit line.

5. (original) The 2-bit non-volatile memory transistor of Claim 4, wherein a portion of the first floating gate electrode is located over the first oxide region, and a portion of the second floating gate electrode is located over the second oxide region.

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6. (original) The 2-bit non-volatile memory transistor of Claim 5, further comprising:

a first oxide layer located on an edge of the first floating gate electrode located over the first oxide region; and

a second oxide layer located on an edge of the second floating gate electrode located over the second oxide region.

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9. (original) The 2-bit non-volatile memory transistor of Claim 1, wherein the control gate comprises polysilicon and metal silicide.

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10. (original) The 2-bit non-volatile memory transistor of Claim 1, wherein the gate dielectric layer comprises silicon oxide, and the dielectric layer comprises a first silicon oxide layer, a silicon nitride or silicon oxynitride layer located over the first silicon oxide layer, and a second silicon oxide layer located over the silicon nitride or silicon oxynitride layer.

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18. (original) A two-bit non-volatile memory transistor comprising:

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a semiconductor region;

a first source/drain region located in the semiconductor region;

a second source/drain region located in the semiconductor region, wherein a channel region is located between the first and second source/drain regions;

a gate dielectric layer located over the channel region and portions of the first and second source/drain regions;

a first floating gate electrode located on the gate dielectric layer over the channel region and the first source/drain region;

a second floating gate electrode located on the gate dielectric layer over the channel region and the second source/drain region, wherein the first and second floating gate electrodes are separated by a gap over the channel region;

a dielectric layer located over a first sidewall and an upper surface of the first floating gate electrode and over a first sidewall and an upper surface of the second floating gate electrode;

a first sidewall oxide region, having a different composition than the dielectric layer, located on a second sidewall of the first floating gate electrode;

a second sidewall oxide region, having a different composition than the dielectric layer, located on a second sidewall of the second floating gate electrode; and

a control gate located over the dielectric layer, the first sidewall oxide region and the second sidewall oxide region.

19. (original) The two-bit non-volatile memory transistor of Claim 18, wherein the dielectric layer comprises silicon nitride.

20. (original) The two-bit non-volatile memory transistor of Claim 19, wherein the dielectric layer further comprises silicon oxide.

21. (original) The two-bit non-volatile memory transistor of Claim 20, wherein the dielectric layer is an oxide-nitride-oxide (ONO) structure.

22. (original) The two-bit non-volatile memory transistor of Claim 18, wherein the first sidewall of the first floating gate electrode and the first sidewall of the second floating gate electrode define portions of the gap.

23. (original) The two-bit non-volatile memory transistor of Claim 18, wherein the first and second floating gate electrodes comprise polysilicon.

24. (original) The two-bit non-volatile memory transistor of Claim 18, further comprising:

a first diffusion bit line continuous with the first source/drain region; and

a second diffusion bit line continuous with the second source/drain region.

25. (original) The two-bit non-volatile memory transistor of Claim 24, further comprising:

a first oxide region located over the first diffusion bit line; and

a second oxide region located over the second diffusion bit line.

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26. (original) The two-bit non-volatile memory transistor of Claim 25, wherein a portion of the first floating gate electrode is located over the first oxide region, and a portion of the second floating gate electrode is located over the second oxide region.

27. (original) The two-bit non-volatile memory transistor of Claim 18, wherein the control gate comprises polysilicon and metal silicide.

28. (original) The two-bit non-volatile memory transistor of Claim 18, wherein the gate dielectric layer comprises silicon oxide.